REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Added device type 09. Redrew entire document.	96-09-27	K. Cottongim

REV																				
SHEET																				
REV	A	A	A	A	A	A														
SHEET	15	16	17	18	19	20														

REV STATUS OF SHEETS															
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
93-04-01

REVISION LEVEL
A

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216

MICROCIRCUIT, HYBRID, MEMORY, DIGITAL, STATIC RANDOM ACCESS MEMORY, CMOS, 256K x 8-BIT

SIZE	CAGE CODE	
A	**67268**	**5962-93157**

SHEET 1 OF 20

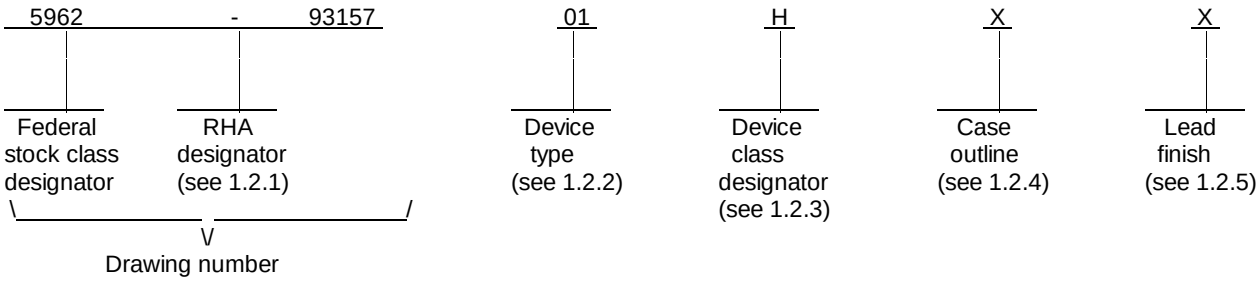
DESC FORM 193
JUL 94

5962-E556-96

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). This drawing describes device requirements for hybrid microcircuits to be processed in accordance with MIL-PRF-38534. Two product assurance classes, military high reliability (device class H) and space application (device class K) and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of radiation hardness assurance levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. Device classes H and K RHA marked devices shall meet the MIL-PRF-38534 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	WS256K8-120CQ	SRAM, 256K x 8-bit	120 ns
02	WS256K8-100CQ	SRAM, 256K x 8-bit	100 ns
03	WS256K8-85CQ	SRAM, 256K x 8-bit	85 ns
04	WS256K8-70CQ	SRAM, 256K x 8-bit	70 ns
05	WS256K8-55CQ	SRAM, 256K x 8-bit	55 ns
06	WS256K8-45CQ	SRAM, 256K x 8-bit	45 ns
07	WS256K8-35CQ	SRAM, 256K x 8-bit	35 ns
08	WS256K8-25CQ	SRAM, 256K x 8-bit	25 ns
09	WS265K8-20CQ	SRAM, 256K x 8-bit	20 ns

1.2.3 Device class designator. This device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
H or K	Certification and qualification to MIL-PRF-38534

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	32	Dual-in-line, dual cavity

1.2.5 Lead finish. The lead finish shall be as specified in MIL-PRF-38534 for classes H and K. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
Signal voltage range (any pin)	-0.5 V dc to +7.0 V dc
Power dissipation (P_D)	1 W
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Input low voltage range (V_{IL})	-0.5 V dc to +0.8 V dc
Input high voltage range (V_{IH})	+2.2 V dc to V_{CC} +0.3 V dc
Output low voltage, maximum (V_{OL})	+0.4 V dc
Output high voltage, minimum (V_{OH})	+2.4 V dc
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbook. Unless otherwise specified, the following specification, standards, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

PERFORMANCE

MIL-PRF-38534 - Hybrid Microcircuits, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Microcircuit Drawings.

(Copies of the specification, standards, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38534 and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38534 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 3.

3.2.4 Timing diagram(s). The Timing diagram(s) shall be as specified on figures 4 and 5.

3.2.5 Block diagram. The block diagram shall be as specified on figure 6.

3.2.6 Output load circuit. The output load circuit shall be as specified on figure 7.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full specified operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38534. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in QML-38534.

3.6 Manufacturer eligibility. In addition to the general requirements of MIL-PRF-38534, the manufacturer of the part described herein shall maintain the electrical test data (variables format) from the initial quality conformance inspection group A lot sample, produced on the certified line, for each device type listed herein. The data should also include a summary of all parameters manually tested, and for those which, if any, are guaranteed. This data shall be maintained under document revision level control by the manufacturer and be made available to the preparing activity (DSCC-VA) upon request.

3.7 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to supply to this drawing. The certificate of compliance submitted to DSCC-VA shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38534 and the requirements herein.

3.8 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38534 shall be provided with each lot of microcircuits delivered to this drawing.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38534.

4.2 Screening. Screening shall be in accordance with MIL-PRF-38534. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition B. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A as specified in accordance with table I of method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V dc $+4.5$ V dc $\le V_{CC} \le +5.5$ V dc unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
DC PARAMETERS							
Supply current	I_{CC}	$\overline{CS} = V_{IL}$, $\overline{OE} = V_{IH}$, duty cycle = $1/t_{RC}$, $V_{CC} = +5.5$ V dc	1, 2, 3	01,02 03 04 05 06,07, 08,09		70 80 90 130 150	mA
Standby current	I_{SB}	$\overline{CS} = V_{CC}$, $\overline{OE} = V_{IH}$, duty cycle = $1/t_{RC}$, $V_{CC} = +5.5$ V dc	1, 2, 3	01,02 03 04 05-09		1.5 2.5 30 50	mA
Input leakage current	I_{LI}	$V_{CC} = +5.5$ V dc, V_{IN} = GND or V_{CC}	1, 2, 3	All		10	µA
Output leakage current	I_{LO}	$\overline{CS} = \overline{OE} = V_{IH}$, V_{OUT} = GND to V_{CC}, $V_{CC} = +5.5$ V dc	1, 2, 3	All		10	µA
Input low voltage	V_{IL}		1, 2, 3	All		0.8	V
Input high voltage	V_{IH}		1, 2, 3	All	2.2		V
Output low voltage	V_{OL}	Device types 01 through 06, $I_{OL} = +2.1$ mA, $V_{CC} = +4.5$ V Device types 07, 08, and 09 $I_{OL} = +8.0$ mA, $V_{CC} = +4.5$ V	1, 2, 3	All		0.4	V
Output high voltage	V_{OH}	Device types 01 through 06, $I_{OH} = -1.0$ mA, $V_{CC} = +4.5$ V Device types 07, 08, and 09 $I_{OH} = -4.0$ mA, $V_{CC} = +4.5$ V	1, 2, 3	All	2.4		V
DATA RETENTION							
Data retention supply voltage	V_{DR}	$\overline{CS} \ge V_{CC} - 0.2$ V	1,2,3	All	2.0	5.5	V

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V dc $+4.5$ V dc $\le V_{CC} \le +5.5$ V dc unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
DATA RETENTION - Continued.							
Data retention current	I_{CCDR}	$V_{CC} = 3.0$ V	1, 2, 3	01-03		1.0	mA
				04		2.0	
				05		4.0	
				06,07, 08,09		6.4	
FUNCTIONAL TESTING							
Functional tests		See 4.3.1c	7,8A,8B	All			
READ CYCLE AC TIMING							
Input capacitance 2/	C_{IN}	$V_{IN} = 0$ V dc, f = 1 MHz	4	All		40	pF
Output capacitance 2/	C_{OUT}	$V_{OUT} = 0$ V dc, f = 1 MHz	4	All		40	pF
Read cycle time	t_{RC}	See figure 4	9,10,11	01	120		ns
				02	100		
				03	85		
				04	70		
				05	55		
				06	45		
				07	35		
				08	25		
				09	20		
Address access time	t_{AA}	See figure 4	9,10,11	01		120	ns
				02		100	
				03		85	
				04		70	
				05		55	
				06		45	
				07		35	
				08		25	
				09		20	
Chip select access time	t_{ACS}	See figure 4	9,10,11	01		120	ns
				02		100	
				03		85	
				04		70	
				05		55	
				06		45	
				07		35	
				08		25	
				09		20	
Output hold from address change	t_{OH}	See figure 4	9,10,11	01,02,03	15		ns
				04	5		
				05-09	3		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V dc +4.5 V dc $\le V_{CC} \le$ +5.5 V dc unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
READ CYCLE AC TIMING - Continued.							
Chip select to output in low impedance	t_{CLZ}	See figure 4	9,10,11	01,02,03	10		ns
				04,05,	5		
				06-09	3		
Chip select to output in high impedance	t_{CHZ}	See figure 4	9,10,11	01, 02		50	ns
				03		45	
				04		40	
				05		35	
				06		30	
				07		20	
				08		17	
				09		15	
Output enable to output valid	t_{OE}	See figure 4	9,10,11	01, 02		60	ns
				03		55	
				04		50	
				05		40	
				06		35	
				07		25	
				08		20	
				09		10	
Output enable to output in low impedance	t_{OLZ}	See figure 4	9,10,11	01-04	5.0		ns
				05-09	0		
Output enable to output in high impedance	t_{OHZ}	See figure 4	9,10,11	01, 02		50	ns
				03		45	
				04		40	
				05		30	
				06		25	
				07		20	
				08		15	
				09		12	
WRITE CYCLE AC TIMING							
Address setup time	t_{AS}	See figure 5	9,10,11	All	2		ns
Write cycle time	t_{WC}	See figure 5	9,10,11	01	120		ns
				02	100		
				03	85		
				04	70		
				05	55		
				06	45		
				07	35		
				08	25		
				09	20		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V dc +4.5 V dc $\le V_{CC} \le$ +5.5 V dc unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
WRITE CYCLE AC TIMING - Continued.							
Write pulse width	t_{WP}	See figure 5	9,10,11	01 02 03 04, 05 06 07 08 09	80 70 65 40 30 25 20 16		ns
Write recovery time	t_{WR}	See figure 5	9,10,11	All	2		ns
Write enable to output in low impedance 2/	t_{WLZ}	See figure 5	9,10,11	01-03 04-09	5 3		ns
Write enable to output in high impedance 2/	t_{WHZ}	See figure 5	9,10,11	01, 02 03 04 05 06 07 08 09	0 0 0 0 0 0 0 0	50 45 40 30 25 20 15 12	ns
Data valid to end of write	t_{DW}	See figure 5	9,10,11	01, 02 03 04 05 06 07 08, 09	50 45 40 30 25 20 15		ns
Data hold time	t_{DH}	See figure 5	9,10,11	01-04 05-09	0 1		ns
Output active from end 2/ of WE	t_{OW}	See figure 5	9,10,11	01-04 05-08 09	10 5 4		ns
Address valid to end of write	t_{AW}	See figure 5	9,10,11	01 02, 03 04, 05 06 07 08 09	85 75 50 30 25 20 16		ns

See footnotes at end of table

TABLE I. Electrical performance characteristics - Continued.

1/ Unless otherwise specified; the AC test conditions are as follows:
Input pulse levels: V_{IL} = 0 V and V_{IH} = 3.0 V.
Input rise and fall times: 5 nanoseconds
Input and output timing reference levels: 1.5 V.
Output loading: See figure 7.

2/ Parameters shall be tested as part of device characterization and after design and process changes. Parameters shall be to the limits specified in table I for all lots not specifically tested.

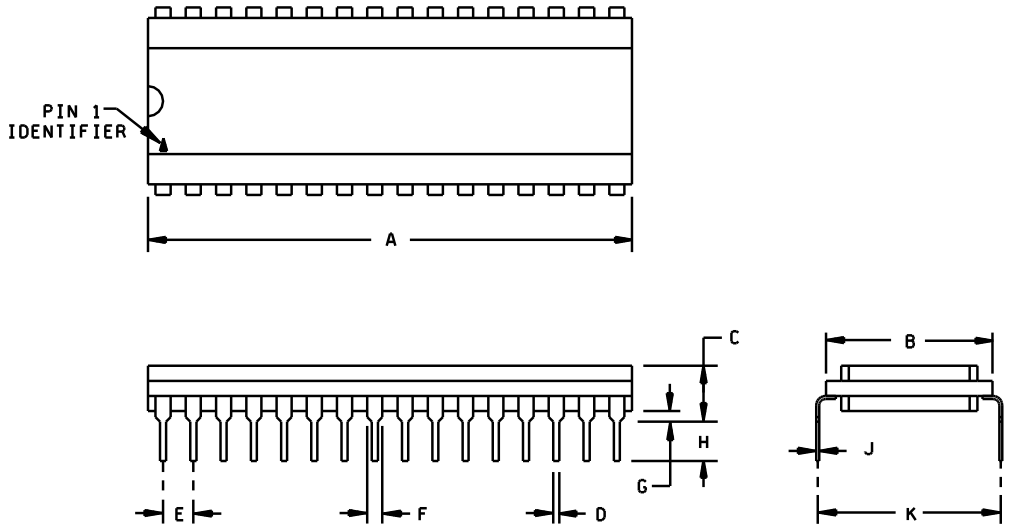


FIGURE 1. Case outlines.

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	40.23	41.05	1.584	1.616
B	13.81	14.12	0.544	0.556
C	3.68	5.08	0.145	0.200
D	0.40	0.51	0.016	0.020
E	2.54 TYP		0.100 TYP	
F	1.14	1.40	0.045	0.055
G	0.64	1.52	0.025	0.060
H	3.18 MIN		0.125 MIN	
J	0.23	0.30	0.009	0.012
K	14.99	15.49	0.590	0.610

FIGURE 1. Case outline - Continued.

Device types	01-09
Case outline	X
Terminal number	Terminal connection
1	NC
2	A16
3	A14
4	A12
5	A7
6	A6
7	A5
8	A4
9	A3
10	A2
11	A1
12	A0
13	I/O 0
14	I/O 1
15	I/O 2
16	V_{SS}
17	I/O 3
18	I/O 4
19	I/O 5
20	I/O 6
21	$\overline{I/O}$ 7
22	CS
23	$\overline{A1}$0
24	OE
25	A11
26	A9
27	A8
28	$\overline{A13}$
29	WE
30	A17
31	A15
32	V_{CC}

FIGURE 2. Terminal connections.

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	AO-A17	Mode	Data I/O	Device
H	X	X	X	Standby	High Z	Standby
L	L	H	Stable	Read	Data out	Active
L	X	L	Stable	Write	Data in	Active
L	H	H	Stable	Output disable	High Z	Active

NOTES:
1. H = VIH = High Logic Level
2. L = V_{IL} = Low Logic Level
3. X = Do not care (either high or low)
4. High Z = High Impedance State

FIGURE 3. Truth table.

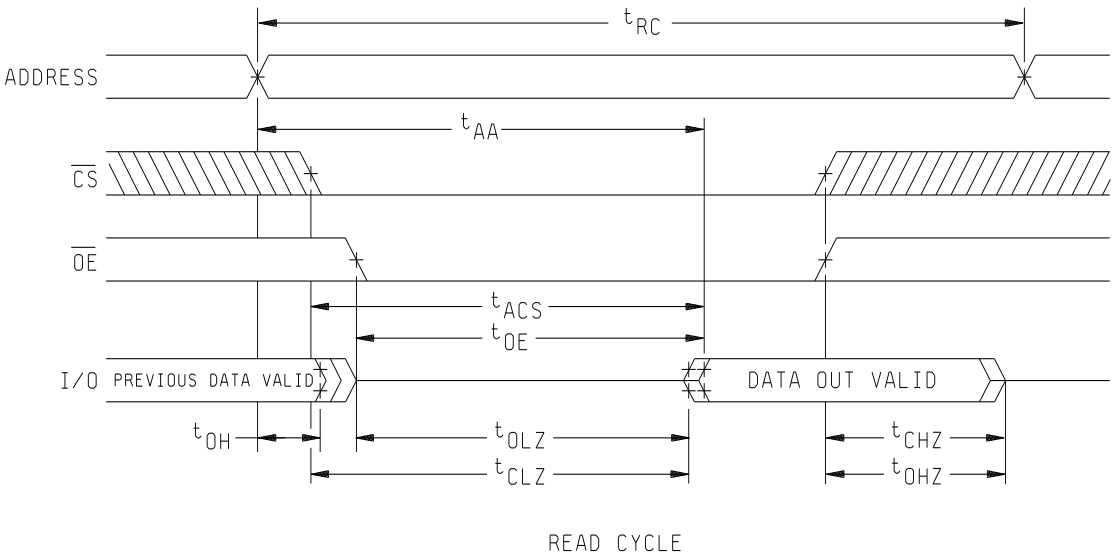
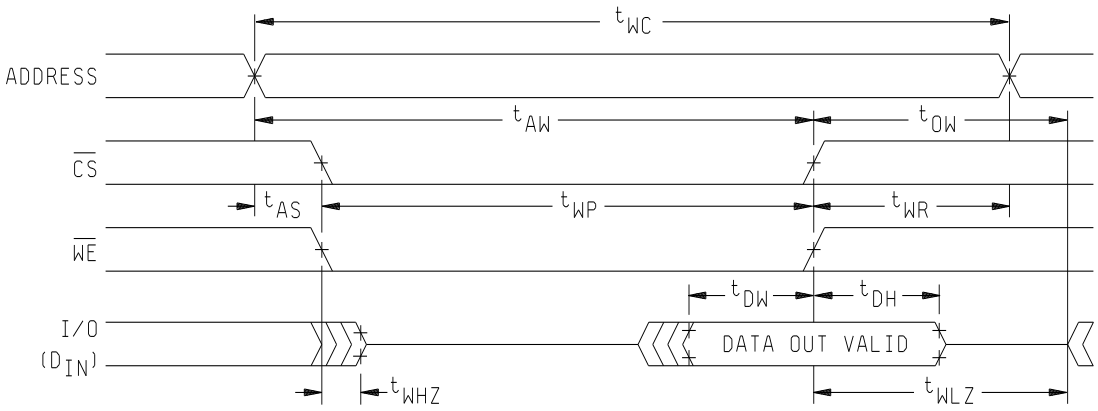


FIGURE 4. Read cycle timing diagram.



WRITE CYCLE

FIGURE 5. Write cycle timing diagram.

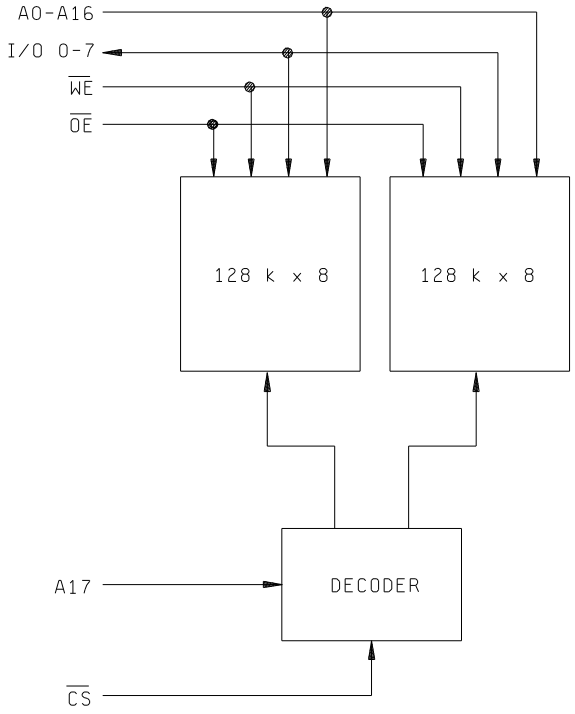
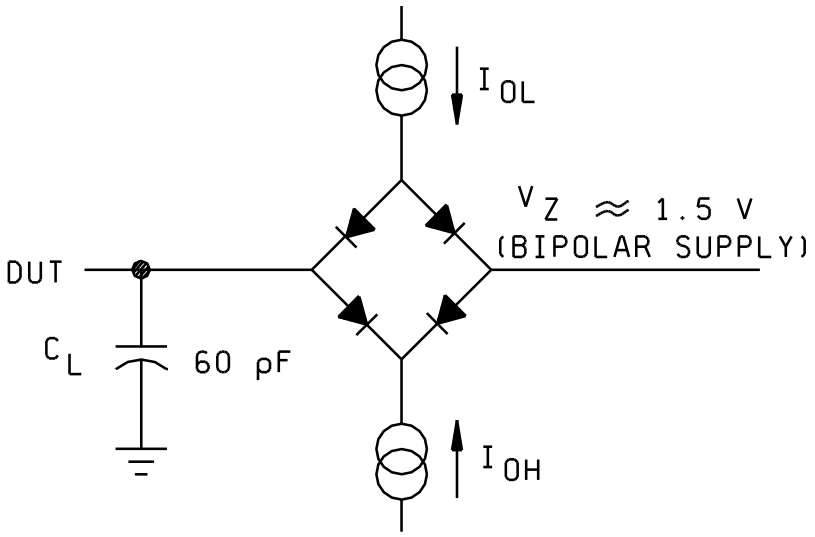


FIGURE 6. Block diagram.



NOTES:
1. V_Z is programmable from -2 V to + 7 V. I_{OH} and I_{OL} are programmable from 0 to 16 mA.
2. Tester impedance, Z_O = 75 ohms.
3. V_Z is typically the midpoint of V_{OH} and V_{OL}, approximately 1.5 V.
4. C_L includes tester jig capacitance.

FIGURE 7. Output load circuit.

TABLE II. Electrical test requirements.

MIL-PRF-38534 test requirements	Subgroups (in accordance with MIL-PRF-38534, group A test table)
Interim electrical parameters	1, 4, 7, 9
Final electrical test parameters	1*, 2, 3, 4, 7*, 8A, 8B, 9, 10, 11
Group A test requirements	1, 2, 3, 4, 7, 8A, 8B, 9, 10, 11
Group C end-point electrical parameters	1, 2, 3, 4, 7, 8A, 8B, 9, 10, 11
MIL-STD-883, Group E end-point electrical parameters for RHA devices	Subgroups ** (in accordance with method 5005, group A test table)

* PDA applies to subgroups 1 and 7.
** When applicable to this standard microcircuit drawing, the subgroups shall be defined.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-PRF-38534 and as specified herein.

4.3.1 Group A inspection. Group A inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 shall be omitted.

c. Subgroups 7, 8A, and 8B shall include verification of the truth table on figure 3.

4.3.2 Group B inspection. Group B inspection shall be in accordance with MIL-PRF-38534.

4.3.3 Group C inspection. Group C inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test, method 1005 of MIL-STD-883.

(1) Test condition B. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A as specified in accordance with table I of method 1005 of MIL-STD-883.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.3.4 Group D inspection. Group D inspection shall be in accordance with MIL-PRF-38534.

4.3.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes H and K shall be M, D, R, and H. RHA quality conformance inspection sample tests shall be performed at the RHA level specified in the acquisition document.

a. RHA tests for device classes H and K for levels M, D, R, and H shall be performed through each level to determine at what levels the devices meet the RHA requirements. These RHA tests shall be performed for initial qualification and after design or process changes which may affect the RHA performance of the device.

b. End-point electrical parameters shall be as specified in table II herein.

c. Prior to total dose irradiation, each selected sample shall be assembled in its qualified package. It shall pass the specified group A electrical parameters in table I for subgroups specified in table II herein.

d. For device classes H and K, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38534 for RHA level being tested, and meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25° C ±5 percent, after exposure.

e. Prior to and during total dose irradiation testing, the devices shall be biased to establish a worst case condition as specified in the radiation exposure circuit.

f. For device classes H and K, subgroups 1 and 2 in table V, method 5005 of MIL-STD-883 shall be tested as appropriate for device construction.

g. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38534.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0526.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000 or telephone (614) 692-0512.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirements documents (MIL-PRF-38534, MIL-PRF-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-PRF-38534 Standard Microcircuit Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-PRF-38535 Standard Microcircuit Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standard Microcircuit Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply for device classes H and K. Sources of supply for device classes H and K are listed in QML-38534. The vendors listed in QML-38534 have submitted a certificate of compliance (see 3.7 herein) to DSCC-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 96-09-27

Approved sources of supply for SMD 5962-93157 are listed below for immediate acquisition only and shall be added to QML-38534 during the next revision. QML-38534 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of QML-38534.

Standard mcrocircuit drawing PIN	Vendor CAGE number	Vendor similar PIN 1/
5962-9315701HXA	54230	WS256K8-120CQ
5962-9315701HXC	54230	WS256K8-120CQ
5962-9315702HXA	54230	WS256K8-100CQ
5962-9315702HXC	54230	WS256K8-100CQ
5962-9315703HXA	54230	WS256K8-85CQ
5962-9315703HXC	54230	WS256K8-85CQ
5962-9315704HXA	54230	WS256K8-70CQ
5962-9315704HXC	54230	WS256K8-70CQ
5962-9315705HXA	54230	WS256K8-55CQ
5962-9315705HXC	54230	WS256K8-55CQ
5962-9315706HXA	54230	WS256K8-45CQ
5962-9315706HXC	54230	WS-256K8-45CQ
5962-9315707HXA	54230	WS256K8-35CQ
5962-9315707HXC	54230	WS256K8-35CQ
5962-9315708HXA	54230	WS256K8-25CQ
5962-9315708HXC	54230	WS256K8-25CQ
5962-9315709HXA	54230	WS256K8-20CQ
5962-9315709HXC	54230	WS256K8-20CQ

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
54230	White Microelectronics 4246 East Wood Street Phoenix, AZ 85040-1943